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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,712	01/14/2000	Tongbi Jiang	3815US (98-0670)	8743

7590

12/31/2002

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EXAMINER

WARREN, MATTHEW E

ART UNIT PAPER NUMBER

2815

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/483,712

Applicant(s)

JIANG ET AL.

Examiner

Matthew E. Warren

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 October 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Arguments filed on October 2, 2002.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth (US 6,147,413) in view of Lee et al. (US 5,894,107).

Farnworth shows (Fig. 2h) a chip scale package comprising a semiconductor die (1004) having an active surface and a plurality of bond pads (1002). The lower surface of a dielectric element (1006) is attached to a portion of the active surface of the die. The lower surface of a plurality of conductive traces (1016) is attached to the upper surface of the dielectric element. Conductive bond members connect each conductive trace to the bond pads. Carrier bonds (1032) are disposed on an upper surface of the conductive trace. An encapsulating material (1018) is disposed on portions of the die, the dielectric element, the conductive traces, the bond members and a portion of the carrier bond. The dielectric element may be any adhesive including polyamide tape or films (col. 4, lines 1-48). The conductive traces may comprise lead fingers or conductive metal. The conductive bond members may comprise any conventional connecting members including metal, wires, aluminum, TAB or thermocompression

bonds. The carrier bond comprises conduct metal or solder balls. The encapsulating material is a non-conductive material with a low elastic modulus film such as polyamide. The carrier bond has lower portion that is attached to the upper surface of the conductive trace and the encapsulating material is disposed about the lower portion of the carrier bond. Farnworth shows all of the elements of the claims except the discrete conductive bond connecting the conductive trace to the bond pad. Lee et al. shows (fig. 1) a chip-size package in which a conductive trace (76) is spaced from a bond pad. A discrete conductive bond (80) in the form of a wire connects the conductive trace to a bond pad (74) formed on the surface of a semiconductor chip (72). The trace, discrete bond, and chip are encapsulated by epoxy mold (82). This configuration is a lead on chip (LOC) which is a specific type of chip-size package. Chip sized package configurations provide the advantage of smaller packages, better electrical performance, higher package density (col. 1, lines 38-51). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conductive trace configuration of Farnworth by employing a lead on chip configuration as taught by Lee to increase the package density and provide better electrical performance.

Response to Arguments

Applicant's arguments filed with respect to claims 1-20 have been fully considered but they are not persuasive. The applicant primarily asserts that Lee et al. does not provide proper motivation for combining with Farnworth. The examiner

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believes that the motivation for combining is proper and the combined references show all of the elements of the claims. The limitation concerning the discrete conductive bond is not patentably distinguishable over the cited art. Discrete conductive bonds, such as bond wires, are well known in the art. Furthermore, the limitation of the discrete conductive bond is not the claimed novel aspect of the invention. Even in the applicant's own prior art figure 1, bond wires (240) provide electrical connection from the lead fingers to the semiconductor chip. Lee was only cited to teach the well known discrete bond. In fact, the teaching comes from the admitted prior art of Lee. Although Lee has a different configuration and different process from Farnworth, the overall goal is the same; connection of the external component to the semiconductor substrate. Lee provides the connection using a discrete bond and shows that such a configuration has benefits. Thus, motivation is shown. For these reasons, the cited art shows all of the elements of the claims and this action is made **final**.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW
MEW
December 30, 2002


EDDIE LEE
SUPERVISOR, PATENT EXAMINER
TECHNOLOGY CENTER